WHAT IS CLAIMED IS:

1. An input/output hub, comprising:

an inbound ordering queue (IOQ) to receive inbound transactions, wherein all read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination;

an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ;

an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write;

an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ; and an unordered domain to receive the inbound transactions transmitted from the IOQ and to receive the outbound transactions transmitted from an unordered protocol.

2. The input/output hub according to claim 1, wherein the IOQ does not permit the inbound read and write transactions to bypass inbound write data.

3. The input/output hub according to claim 1, wherein the unordered protocol is a coherence interface.

4. The input/output hub according to claim 3, wherein the coherent interface is a Scalability Port.

5. An input/output hub, comprising:

an ordered domain, including:

an inbound ordering queue (IOQ) to receive and transmit inbound transactions, wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination,

an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ,

an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write, and

an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ; and

an unordered domain, in communication with an unordered protocol, including:

an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol, and

an outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain.

6. The input/output hub according to claim 5, further including at least one Producer-Consumer ordered interface in communication with the ordered domain.

7. The input/output hub according to claim 6, further including an input/output device connected with the Producer-Consumer ordered interface.

8. The input/output hub according to claim 7, further including an intermediary device interconnecting the Producer-Consumer ordered interface and an input/output device.

9. The input/output hub according to claim 7, wherein the input/output device is a Peripheral Component Interconnect (PCI) device.

10. The input/output hub according to claim 5, wherein the unordered protocol is a coherence interface.

11. The input/output hub according to claim 10, wherein the coherent interface is a Scalability Port.

12. An input/output system, comprising:

an ordered domain, including:

an inbound ordering queue (IOQ) to receive and transmit inbound transactions, wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination;

an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ,

an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write,

an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ;

an unordered domain, in communication with an unordered protocol, including:

an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol, and

an outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain;

a Producer-Consumer ordered interface in communication with the ordered domain;

an input/output device connected with the Producer-Consumer ordered interface; and

a coherent interface within the unordered protocol in communication with the unordered domain.

13. The input/output system according to claim 12, wherein the coherent interface is a Scalability Port.

14. The input/output system according to claim 12, wherein the input/output device is a Peripheral Component Interconnect (PCI) device.

15. The input/output system according to claim 12, further including an intermediary device interconnecting the Producer-Consumer ordered interface and the input/output device.

16. An input/output system, comprising:

an ordered domain having a first functional block and a second functional block, wherein the first functional block and the second functional block each include:

an inbound ordering queue (IOQ) to receive inbound transactions, wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes

in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination,

an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ,

an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write,

an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ;

an unordered domain, in communication with an unordered protocol, including:

an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol, and

an outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain;

a first Producer-Consumer ordered interface in communication with the first functional block;

a first input/output device connected with the first Producer-Consumer ordered interface;

a second Producer-Consumer ordered interface in communication with the second functional block;

a second input/output device connected with the second Producer-Consumer ordered interface; and

a coherent interface within the unordered protocol in communication with the unordered domain.

17. The input/output system according to claim 16, wherein the coherent interface is a Scalability Port

18. The input/output system according to claim 16, wherein the first input/output device is a Peripheral Component Interconnect (PCI) device.

19. The input/output system according to claim 16, wherein the second input/output device is a Peripheral Component Interconnect (PCI) device.

20. The input/output system according to claim 16, further including a first intermediary device interconnecting the first Producer-Consumer ordered interface and the first input/output device.

21. The input/output system according to claim 16, further including a second intermediary device interconnecting the second Producer-Consumer ordered interface and the second input/output device.

22. A computer system, comprising:

a plurality of processor units having access to caches;

a main memory;

a coherent interface to maintain coherency between the processor units and their caches;

a scalability node controller interconnecting the processor units, the main memory, and the coherent interface to control interface therebetween; and

an input/output hub in communication with the coherent interface, including:

an inbound ordering queue (IOQ) to receive inbound transactions, wherein all read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination;

an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ;

an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write;

an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ; and

an unordered domain to receive the inbound transactions transmitted from the IOQ and to receive the outbound transactions from the coherent interface.

23. The computer system according to claim 22, wherein the IOQ does not permit the inbound read and write transactions to bypass inbound write data.

24. The computer system according to claim 22, wherein the coherence interface is an unordered protocol.

25. The computer system according to claim 22, wherein the coherent interface is a Scalability Port.